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Guide to Spintronic Crossbar Arrays: From Binary Switches to Analog Computing

Pietro Perlo*

Interactive Fully Electrical VehicleS (IFEVS), La Loggia, Italy

*Corresponding Author: Pietro Perlo, Interactive Fully Electrical VehicleS (IFEVS), La Loggia, Italy.

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Abstract

Spintronic crossbar arrays are emerging as a powerful hardware platform for energy-efficient computing. Unlike conventional digital processors that shuttle data between memory and processing units, these arrays perform computation directly where data is stored, a concept known as in-memory computing. This report explains, from the ground up, what spintronic crossbars are, how they operate, and the different types currently available or under development. We cover both binary (single-level) and analog (multi-level) devices, their input/output characteristics, and the physical principles that make them uniquely suited for matrix operations. The figures illustrate the architecture, switching mechanisms, and the transition from binary to multi-level behavior. This foundation is essential for understanding advanced applications such as parallel photovoltaic MPPT and neuromorphic computing.

Keywords: Spintronic Crossbar Arrays, Magnetic Tunnel Junctions, Mtj, In-Memory Computing, Analog Computing, Matrix-Vector Multiplication, Mram, Binary Crossbar, Multi-Level Devices, Neuromorphic Hardware, Transimpedance Amplifiers, Tunnel Magnetoresistance

Acronym	Meaning
ADC	Analog-to-Digital Converter
IMC	In-Memory Computing
IR drop	Voltage drop caused by line resistance
KCL	Kirchhoff's Current Law
MRAM	Magnetoresistive Random-Access Memory
MTJ	Magnetic Tunnel Junction
MVM	Matrix-Vector Multiplication
RRAM	Resistive Random-Access Memory
TIA	Transimpedance Amplifier
TMR	Tunnel Magnetoresistance

Table

Learning Objectives

Explain how a crossbar performs matrix–vector multiplication using Ohm's law and Kirchhoff's current law.

Describe what a magnetic tunnel junction (MTJ) is and how it stores information (binary and multi-level).

Understand how crossbar outputs are sensed and converted (TIA/ADC) and what limits accuracy (noise, variability, IR drop).

Distinguish between what is commercially available today (MRAM memory products) and what is still mainly at research/prototype stage (analog crossbar computing).

Prerequisites: basic circuit laws (Ohm and Kirchhoff) and the idea of resistance vs conductance.

Roadmap of the lecture sequence. This first note introduces the physical and architectural principles of spintronic crossbars, from MTJ operation to matrix-vector multiplication, readout, and non-idealities. The following notes then build progressively on this foundation: the second presents the classical digital MPPT benchmark for a partially shaded PV string, the third examines a hybrid architecture combining spintronic bypass control with conventional digital MPPT, and the fourth discusses a fully analog spintronic-crossbar control architecture. The present note should therefore be read as the conceptual entry point for the application-oriented lectures that follow.

Introduction: Why Crossbars?

In a conventional computer, the processor and memory are separated. To perform a calculation, data must travel from memory to the processor, be processed, and then travel back. This back and forth, known as the von Neumann bottleneck, limits speed and consumes energy.

To quantify this, the von Neumann bottleneck is essentially a bandwidth limitation. If a processor operates at frequency f and the data bus transfers B bits per cycle, the processor often sits idle waiting for data. In memory computing effectively makes the memory its own processor, eliminating this delay.

A crossbar array offers an alternative. Imagine a grid of wires: horizontal rows and vertical columns. At each intersection, a tiny electronic device connects the row to the column. When voltages are applied to the rows, currents flow through these devices and are collected at the columns. The output currents are the result of a matrix vector multiplication, performed in a single, parallel step. This is the essence of in memory computing.

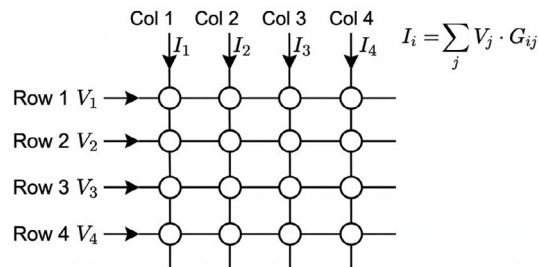


Figure 1: Conceptual Crossbar Array. Input Voltages V_1 – V_4 are Applied to the Horizontal Rows; Output Currents I_1 – I_4 are Collected from the Vertical Columns. The Conductance at Each Intersection G_{ij} Determines How Much Current Flows from a Given Row to a Given Column. The Column Currents are the Weighted Sums of the Row Voltages, Performing a Matrix Vector Multiplication in a Single Analog Step

What is a Spintronic Device?

A spintronic device, short for “spin based electronic device”, uses the quantum spin of electrons, not just their charge, to store and process information. An electron can have two spin states: “spin up” or “spin down.” In a magnetic material, these spin states correspond to different magnetic orientations.

The most common spintronic device for crossbars is the magnetic tunnel junction (MTJ). An MTJ consists of two ferromagnetic layers separated by a thin insulating barrier:

- **Reference Layer:** Fixed magnetization.
- **Free Layer:** Magnetization can be switched.

When the magnetizations of the two layers are aligned (parallel), the resistance is low. When they are opposite (anti parallel), the resistance is high. This difference, called tunnel magnetoresistance (TMR), allows the device to store a binary state (0 or 1). We measure the efficiency of this state change using the TMR ratio, which defines the “read window” or the contrast between our 0s and 1s:

$$\text{TMR} = \frac{R_{\text{AP}} - R_{\text{P}}}{R_{\text{P}}} \times 100\%$$

Plain-text equation: $\text{TMR} = (R_{\text{AP}} - R_{\text{P}}) / R_{\text{P}}$

where R_{P} is the low resistance parallel state and R_{AP} is the high resistance anti parallel state. A higher TMR makes the device more resilient to electronic noise.

This binary state is what gives the crossbar its programmable conductance.

Magnetic Tunnel Junction (MTJ) – Parallel and Anti-Parallel States

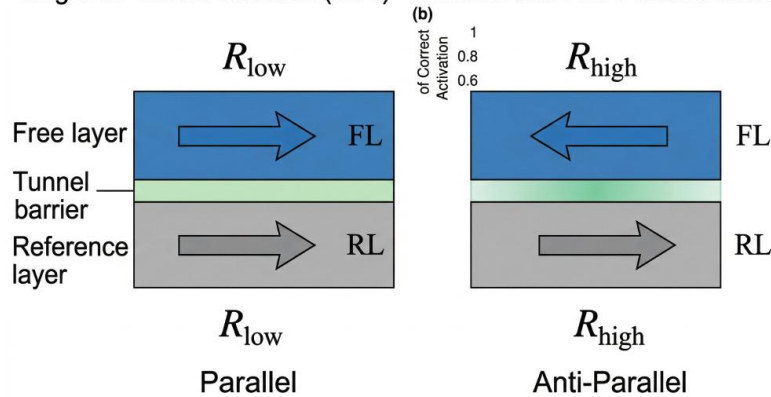


Figure 2: Illustrates an MTJ Structure. Magnetic Tunnel Junction (MTJ). (a) Parallel Magnetization – Low Resistance. (b) Anti Parallel Magnetization – High Resistance. The Tunnel Barrier Separates the two Ferromagnetic Layers

The Crossbar Architecture: Inputs and Outputs

A crossbar array is built by placing spintronic devices at the intersections of perpendicular nanowires. Each intersection is called a crossbar junction. The array has:

- **Rows (word lines):** Carry input voltages. In our context, these are the signals we want to process, for example, sensor voltages.
- **Columns (bit lines):** Carry output currents. These are the results of the computation.
- **Device at (i,j):** Has a programmable conductance G_{ij} . The conductance is set by the state of the spintronic device (binary or multi level).

The output current at column i is the physical result of two fundamental laws of physics working together:

- **Ohm's Law:** Multiplication is performed by the conductance at the junction ($I=V \cdot G$).
- **Kirchhoff's Current Law:** Addition is performed as currents from all rows merge into the column wire.

The total current for any column i is:

$$I_i = \sum_{j=1}^n V_j \cdot G_{ij}$$

Plain-text equation: $I_i = \sum_j (V_j \cdot G_{ij})$ (junction currents summed by KCL along a column)

In matrix form this is the classic Matrix-Vector Multiplication (MVM):

Plain-text matrix form: $I = G \cdot V$ (currents = conductance matrix \times voltage vector)

Mini Example (2x2 Crossbar):

Let the input voltages be $V = [V_1, V_2]^T = [0.20 \text{ V}, 0.10 \text{ V}]^T$.

Let the conductance matrix be $G = [[1 \text{ mS}, 2 \text{ mS}], [0.5 \text{ mS}, 1 \text{ mS}]]$.

Then $I = G \cdot V$ gives:

$$I_1 = (1 \text{ mS})(0.20 \text{ V}) + (2 \text{ mS})(0.10 \text{ V}) = 0.20 \text{ mA} + 0.20 \text{ mA} = 0.40 \text{ mA}$$

$$I_2 = (0.5 \text{ mS})(0.20 \text{ V}) + (1 \text{ mS})(0.10 \text{ V}) = 0.10 \text{ mA} + 0.10 \text{ mA} = 0.20 \text{ mA}$$

Interpretation: the crossbar produces two analog output currents that already contain the multiply–accumulate result.

Important: even if each cell stores only 0/1 (two conductance values), the column output is still an analog current sum. It becomes 'digital' only after sensing and thresholding/ADC.

$$I = V \cdot G$$

Where V is the row voltage vector and G is the conductance matrix.

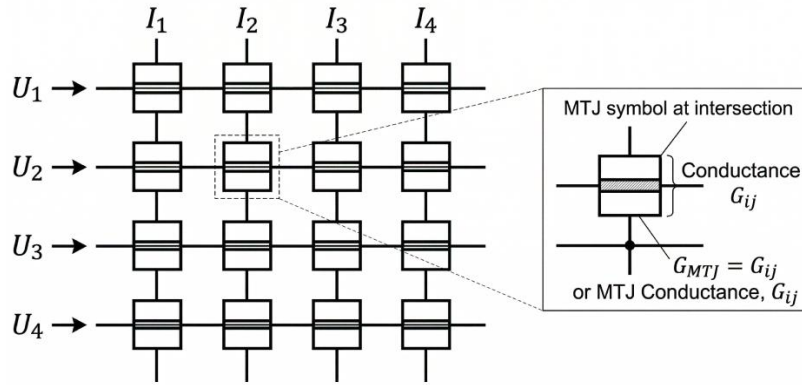


Figure 3: Shows a 4×4 Crossbar Array with Devices at Each Junction. A 4×4 Crossbar Array. Input Voltages (V1–V4) are Applied to Rows. Each Junction Contains a Spintronic Device with Conductance G_{ij} . Output Currents (I1–I4) are the Sum of Contributions from All Rows

Reality check (Non-Idealities in Real Crossbars):

- Wire resistance (IR drop): voltages along a long row are not identical; this distorts the intended V values.
- Sneak paths / leakage: unintended current paths can appear if devices are not well isolated (selector devices help).
- Device variability: 'same' conductance state may vary across cells, limiting accuracy.
- Nonlinearity: conductance may depend on applied voltage and temperature.
- Noise and sensing limits: the readout circuit (TIA/ADC) adds noise and quantization error.
- Finite settling time: parasitic capacitances mean outputs need time to stabilize before sampling.

Binary (Single Level) Operation

In its simplest form, each spintronic device is binary: it can be either in a low resistance state (closed latch) or a high resistance state (open latch). These states represent logic values "1" (low resistance) and "0" (high resistance), respectively.

In this mode, the conductance G_{ij} is a discrete variable restricted to a set of two values:

$$G_{ij} \in \{G_L, G_H\}$$

where G_H (high conductance) represents a logic 1 and G_L (low conductance) represents a logic 0. This makes the array act like a massive parallel "pattern matcher".

In this mode, the conductance G_{ij} is restricted to two values:

$$G_{ij} = \begin{cases} G_{\text{high}} & (\text{logic 1}) \\ G_{\text{low}} & (\text{logic 0}) \end{cases}$$

Switching

The state can be changed by applying a current pulse through the device. If the current exceeds a certain threshold, the magnetization of the free layer flips, changing the resistance. This is done during a programming phase before normal operation.

Advantages of Binary Devices

- **Non volatile:** state is retained without power.
- **Fast:** switching in nanoseconds.
- **Endurance:** virtually unlimited write cycles.

Output: The output current at each column is a weighted sum of the inputs, where the weights are either G_H (representing 1) or G_L (representing 0). This produces a binary weighted analog output. For example, if we set $G_H=100 \mu\text{S}$ and $G_L=1 \mu\text{S}$, then the output is a sum of the input voltages multiplied by either 100 or 1, depending on the stored bits.

Note: the crossbar itself is still performing analog physics. 'Binary' here refers to the stored weight levels (two conductances). To use the result in digital logic, we sense the column current and output using a comparator or ADC.

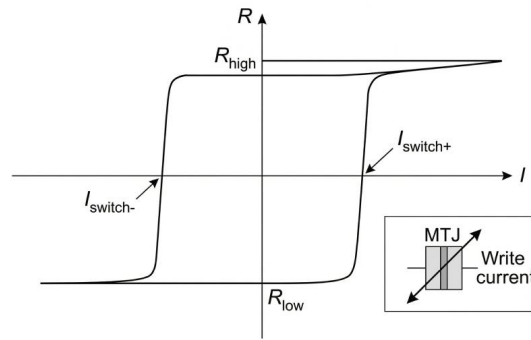


Figure 4: Shows The Binary Switching Characteristic. Binary Switching of an mtj. A Current Pulse Above Threshold Switches the Device from High Resistance (r_high) to Low Resistance (r_low). The Inset Shows the Hysteresis Loop of Magnetization

Multi Level (Analog) Operation

Binary devices store only one bit per cell. For applications that require continuous weight values, such as neural networks or advanced control algorithms, multi level devices are needed. In a multi level spintronic crossbar, each device can have more than two distinct conductance levels, allowing it to represent a continuous analog value.

How It Works

Instead of having a uniform free layer that switches all at once, a multi level MTJ uses a granular nanostructure. The free layer consists of many small magnetic grains (8–10 nm) that switch at slightly different currents. As the programming current increases, more grains switch, and the overall resistance changes in small steps.

The “analog” behavior in granular MTJs is actually the statistical sum of many microscopic magnetic flips. If a device contains N grains, the total conductance “ G ” is approximately the sum of all grains that have been switched to the parallel state:

$$G_{\text{total}} \approx \sum_{k=1}^N \text{state}_k \cdot g_k$$

where g_k is the conductance contribution of a single grain and $\text{state}_k \in \{0,1\}$ indicates whether that grain is in the parallel state. This allows us to map digital “weights” (like those in a neural network) to specific physical conductance levels.

By carefully controlling the current pulse amplitude, any intermediate resistance can be set.

State Of The Art

Research has demonstrated up to 2 bits per cell (4 levels) reliably, and development is ongoing toward 4 bits per cell (16 levels). These multi level devices are still in the research phase, but they hold great promise for true analog computing.

Output

In a multi level crossbar, each conductance G_{ij} can take one of many values (e.g., 16 levels). The output current at column i is still $I_i = \sum_j V_j \cdot G_{ij}$, but now the weights are continuous, allowing precise analog computations.

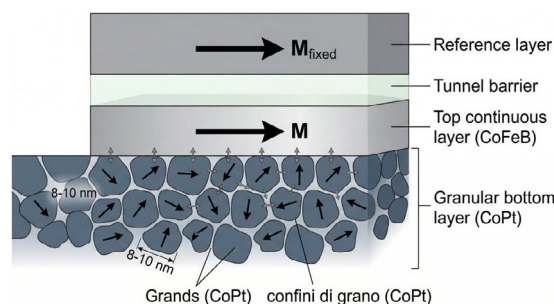


Figure 5: Illustrates the Granular Nanostructure. Granular Nanostructure for Multi Level MTJ. Bottom Granular Layer (CoPt alloy) with Magnetic Grains (8–10 nm). Top Continuous Layer (CoFeB) Coupled via Exchange. The Magnetization of the top Layer Follows the Average of the Bottom Grains, Enabling Intermediate States

Programming the Crossbar

To use a crossbar for a specific computation, we must first set the conductances G_{ij} to the desired values. This is done during a programming phase, separate from the normal operation. For binary crossbars, programming is simply writing bits (0 or 1) into each cell using current pulses. For multi level crossbars, we apply precisely controlled current pulses to achieve the desired intermediate conductance.

Practical Note (Multi-Level Weights): programming is usually iterative ("program-and-verify"). A controller applies a short pulse, reads the resulting conductance, and repeats until the target level is reached within tolerance. This compensates for device variability and drift.

Once programmed, the crossbar acts as a fixed analog computing engine. The input voltages are applied to the rows, and the output currents appear at the columns in nanoseconds. No further programming is needed until we want to change the function.

In this report, we do not go into the details of how the programming circuits are designed or the specific materials used. Instead, we focus on the fundamental operation: inputs (voltages on rows), outputs (currents on columns), and the role of the programmed conductances.

What the Crossbar Reads and Outputs

Inputs

- **Rows:** Analog voltages (continuous values) or digital voltages (binary). These are the signals we want to process, for example, sensor readings, cell voltages, or control signals.
- **Programming:** During programming, current pulses are applied to set the conductances. This is done once before operation.

Outputs

- **Plain-Text Equation:** $I_i = \sum_j (V_j \cdot G_{ij})$ (junction currents summed by KCL along a column)
- **Columns:** Analog currents, given by $I_i = \sum_j V_j \cdot G_{ij}$.
- **Binary Case:** Output is a weighted sum with binary weights (either G_H or G_L).
- **Multi level Case:** Output is a true analog weighted sum with continuous weights.

How outputs are sensed (readout electronics):

- Column outputs are currents. In hardware, we normally convert them to voltages using a transimpedance amplifier (TIA) or a resistor, then digitize.
- Typical signal chain: Crossbar column current \rightarrow TIA ($I \rightarrow V$) \rightarrow anti-alias filter (optional) \rightarrow ADC \rightarrow digital code.
- ADC requirements depend on the number of distinct output levels and on noise/variability. Multi-level weights usually require higher effective resolution than binary weights.

The outputs can be:

- Directly used as control signals (e.g., to trigger comparators).
- Converted to digital via ADCs for further processing. The resolution of the Analog to Digital Converter (ADC) must match the precision of the crossbar. For example:

A binary crossbar only needs a 1 bit ADC (a simple comparator).

A 16 level crossbar (4 bit precision) requires at least a 4 bit ADC to accurately distinguish between the possible output states.

- Fed into another crossbar for multi layer computations.

Types of Spintronic Crossbars: State of the Art

Type	Device	Levels	Output	Status	Reference
Binary STT MRAM	Standard MTJ	2	Binary weighted analog	Commercial	[1] (overview of spintronic memristors) or product datasheet
Multi level STT MRAM	Granular MTJ	4+	Continuous analog	Research	[2] (Gupte et al., npj Unconventional Computing, 2026)
SOT MRAM	MTJ with heavy metal	2	Binary weighted analog	Emerging	[3] (Zvezdin, SpinEdge seminar, 2025) or [4] (Deng et al., Advanced Functional Materials, 2024)

Domain Wall	MTJ with extended track	Multiple	Analog	Research	[1] (general spintronics review) or classic reference (e.g., Parkin et al., Science, 2008)
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Binary STT MRAM

- Mature technology already in production.
- High density, good endurance, CMOS compatible.
- Used for embedded memory and in memory computing.

Multi Level Granular MTJ

- Novel structure using granular nanostructures.
- Near continuous states without special lithography.
- Enables analog synaptic weights for neuromorphic computing.

Spin Orbit Torque (SOT) Devices

- Three terminal configuration: separate read and write paths.
- Faster writing, lower power, but larger area.
- Can also be adapted for multi level operation.

Domain Wall Devices

- Use motion of magnetic domain walls along a track.
- Multiple states by positioning the wall.
- Require special geometry (e.g., notches, curved tracks).

Commercial Status: What Exists today (Binary vs Multi-Level)

Binary (Commercially Available)

spintronic memory (MRAM, especially STT-MRAM) is a mature product category. Several vendors sell MRAM memory chips that use binary MTJs (two stable resistance states), mainly as non-volatile embedded or stand-alone memory. These parts are 'spintronic' and are commercially available, but they are sold as memory, not as analog matrix-multiply accelerators [5,6].

Compute-in-Memory (Prototype Demos)

Major semiconductor groups have demonstrated MRAM-based in-memory computing macros (using MRAM arrays plus sensing circuits) to accelerate multiply-accumulate operations. This shows a technology path from commercial MTJ memory toward computing arrays, but these are still closer to advanced prototypes than mass-market products [7].

Multi-level (Mostly Research)

Robust multi-bit MTJ 'synapses' and true analog crossbar computing are active research topics. Multi-level operation requires tighter control of device states, programming/verify loops, and higher-precision sensing. For this reason, most multi-level spintronic crossbar results are reported in research papers rather than product datasheets. (See, for example, [4].)

Capability	Description
In memory computing	Compute directly where data is stored, eliminating von Neumann bottleneck. [2], [8], [9]
Parallel operation	All rows and columns active simultaneously.
Matrix vector multiplication	$I=U \times G$ in nanoseconds.
Binary or analog	Single level (binary) or multi level (continuous) weights.
Non volatile	States retained without power.
Reconfigurable	Program G matrix for different functions.

Summary: What a Spintronic Crossbar Can Do

Current Limitations and Recent Advances

While spintronic crossbars promise exceptional speed and energy efficiency, they are not yet "perfect components." Real designs must account for temperature dependence, manufacturing variability, stability (especially for multi-level states), and array-level non-idealities such as IR drop and sneak-path currents. The good news is that many of these limitations are engineering challenges rather than fundamental blockers, and the last few years have delivered major improvements in stability and manufacturability (particularly for perpendicular MTJ stacks and mature MRAM processes).

Temperature Sensitivity

Spintronic devices rely on magnetic ordering, so key parameters drift with temperature. As temperature rises, the tunnel

magnetoresistance (TMR) ratio and the resistance contrast between states typically decrease, reducing read margin. Switching thresholds (critical current/voltage) and retention margins also vary with temperature because they depend on the thermal stability factor. Industrial MRAM products therefore specify retention targets and validate them through high-temperature qualification, showing that stable operation is achievable at scale. For sensing applications, the same MTJ technology is widely used in TMR sensors, where temperature-dependent sensitivity and offset drift are mitigated through calibration and compensation methods (hardware or software). These sensor techniques are directly relevant to crossbar readout and long-term stability management [8,9–12].

Manufacturing Variability and Materials Control

In a crossbar array, each MTJ is fabricated in a dense matrix; even with state-of-the-art lithography there are small variations in film thickness, grain structure, and etch profile across a wafer. Because an MTJ is a nanoscale multilayer (often CoFeB/MgO/CoFeB), the barrier/interface quality strongly affects TMR, resistance-area (RA) product, and switching distributions. These variations broaden the resistance (or conductance) distributions of the nominal 'same' state and can reduce the number of reliably distinguishable levels, especially for multi-level operation. Practical multi-level systems therefore rely on iterative program-and-verify and periodic recalibration to compensate variability and drift [4,8,13,14].

Endurance, Retention, and Read Disturb

MTJs can offer very high write endurance, which is excellent for repeated reprogramming. However, repeated reads can cause read-disturb if the read current is too high; modern sensing schemes keep read currents well below switching thresholds. Retention is the complementary requirement: the stored state (binary or intermediate) must remain stable over time and temperature. Binary MRAM is already qualified for long retention, whereas multi-level analog states require tighter control and often depend on verify/re-write loops to maintain precision [4,9].

Sneak Paths and Selector / Access Devices

In a passive crossbar, every junction shares row and column wires. During read or compute operations, unintended current can flow through neighbouring devices (sneak paths), corrupting the measured output. To mitigate this, many practical arrays use access devices (e.g., 1T-1MTJ in MRAM macros) or selector elements that enforce non-linear I-V behaviour. Selectors add area and complexity but become increasingly important as arrays scale [9,15,16].

IR Drop, Parasitics, Noise, and Crossbar Scaling

When voltages are applied to long rows, currents through the metal lines create voltage gradients (IR drop), so the atrice sint voltage is not atrice sinto the array. Parasitic capacitances set a finite settling time, limiting how quickly outputs can be sampled. Finally, the readout chain (TIA/ADC or comparators) introduces noise and quantization error, which can dominate when conductance differences are small (multi-level operation). Common mitigation strategies include tiling large atrice sinto smaller sub-arrays, adding calibration, and designing sensing circuits matched to the required precision [15,16].

Recent Advances: Why Stability Has Improved

Despite these challenges, the last few years have seen rapid progress that improves stability and practical deployability:

- **Higher TMR and Better Thermal/Anneal Stability:** perpendicular MTJ stacks have demonstrated strong thermal stability at small dimensions and high magnetoresistance, improving sensing margin and robustness [8,9,13,14,].
- **Multi-Level Repeatability:** granular MTJ approaches combined with program-and-verify can achieve tighter level distributions (multi-bit 'synapses'), improving practical analog operation [2].
- **Manufacturing Maturity:** commercial MRAM products and embedded MRAM process options demonstrate that MTJ fabrication can meet industrial reliability targets [5-7,9].
- **Array-level Mitigation:** crossbar-aware circuit techniques (tiling, calibration, access devices/selectors) reduce sneak paths and IR-drop effects in larger arrays [15,16].
- **Spintronics Beyond Crossbars (TMR Sensors):** TMR sensors are widely used in industry and automotive; recent work shows effective temperature compensation (hardware/software), validating long-term stability and manufacturability of MTJ technology [10–12].

Crossbar matrices still face non-idealities, but stability and manufacturability have improved significantly. Binary MRAM is already commercial, and research progress is steadily pushing multi-level crossbars toward practical engineering reality.

Conclusion

Spintronic crossbar arrays represent a fundamental shift in how computation can be performed. By combining storage and processing in a single array, they overcome the von Neumann bottleneck that limits conventional digital systems. Binary devices are already commercial; multi level devices based on granular nanostructures are opening the door to true analog computing, where weights are continuous and matrix operations happen in a single parallel step. The

challenges of temperature sensitivity, variability, and sneak paths have been addressed by advanced materials, selector devices, and iterative programming schemes, leading to rapid adoption of spintronic technology in embedded memory and magnetic sensing. This momentum makes the prospect of large scale analog crossbar computing increasingly realistic.

This foundation is essential for understanding advanced applications, from ultra fast bypass and MPPT in photovoltaic systems to neuromorphic computing and energy harvesting IoT nodes. The same crossbar architecture serves as a versatile platform for intelligent energy management across all scales.

Appendix A. Optional example: Crossbar-Style Computation Inside An Mppt Control Loop

This appendix is included to connect the device- and architecture-level concepts developed in the main text with a representative control problem in energy harvesting, namely photovoltaic maximum-power-point tracking (MPPT) under rapidly varying mismatch conditions. The preceding sections have explained how spintronic crossbars implement parallel matrix-vector operations, how binary and multi-level conductance states can be encoded in MTJ-based devices, and how the resulting analog column currents can be sensed and interpreted. In the present appendix, the same principles are considered at a higher abstraction level in order to illustrate how a programmable crossbar may operate as an analog decision-forming block inside a closed-loop PV control architecture. The purpose is not to present a detailed implementation recipe, but to provide a physically meaningful bridge from crossbar fundamentals to a relevant application domain that motivates the companion notes that follow.

Figure 6 should therefore be interpreted as a system-level conceptual synthesis rather than as a device-level characterization or a fully validated engineering prototype. Its role is to show how the computational primitives introduced earlier in this note, parallel weighted summation, programmable conductance mapping, analog readout, and low-latency decision formation, may be repurposed for photovoltaic mismatch handling and power-control signaling. The four panels are complementary. Panel A summarizes the overall control architecture, in which a 4×4 spintronic crossbar is embedded in a PV control chain. Panel B emphasizes the timing distinction between rapid bypass decision formation and the slower relocking of the operating point imposed by converter and source dynamics. Panel C presents a conceptual benchmark-style summary of latency, energy, and co-optimization considerations. Panel D extends the discussion to an illustrative scaling perspective, suggesting how the same architectural logic may influence larger systems and annual energy yield. Taken together, the figure is intended to help the reader move from the question “what is a spintronic crossbar?” to the more application-oriented question “why might such a crossbar matter in an energy-harvesting system?”

At the level of principle, the crossbar may receive measured inputs such as the individual cell voltages $V_{c1} \dots V_{c4}$, and, where appropriate, selected string-level observables such as V_{string} and I_{string} . A programmed conductance matrix G then defines a linear or approximately linear mapping from these inputs to analog output currents. After suitable interface stages, for example transimpedance conversion, comparator thresholding, or ADC-based observation, these outputs can be interpreted as control-oriented quantities, such as a duty-cycle correction ΔD for the DC-DC converter and/or bypass indicators identifying a cell or subgroup affected by shading-induced mismatch. Importantly, MPPT remains a feedback problem: the physical system must still be measured, the control action must still be applied to the converter, and the resulting operating point must still be re-evaluated. The contribution of the crossbar is therefore not to eliminate the feedback loop, but to reduce the latency and sequential overhead associated with the decision-forming stage by carrying out the relevant weighted-sum operations in parallel. Any digital controller retained in the system may still provide supervisory functions such as safety limits, hysteresis, dwell times, event handling, and PWM update management.

From an energy-harvesting perspective, the interest of this architecture lies in the mechanism by which faster and more parallel decision formation can translate into higher harvested energy, especially under conditions of dynamic shading. In a conventional sequential control chain, a mismatch event is first measured, then digitized, then processed, and only afterward converted into a bypass or converter-control action. During that interval, the shaded cell or substring may remain in a non-optimal operating region, the string may operate away from its best power point, and part of the available irradiance may be dissipated rather than harvested. A crossbar-assisted architecture can, in principle, reduce this inactive interval by forming bypass-related and power-control-related signals in parallel and with very low intrinsic decision latency. The corresponding energy advantage is not the result of a single dramatic event, but of the repeated avoidance of short intervals of suboptimal operation. When partial shading evolves slowly, this advantage may be modest. When mismatch changes frequently, for example under moving shadows, urban driving, roadside vegetation, or vibration-induced illumination changes on mobile photovoltaic surfaces, the cumulative effect can become significant because the controller spends less time reacting and more time operating near a favorable power point.

A second mechanism for improved harvested energy is the tighter coupling between local mismatch awareness and global converter action. In conventional low-channel-count systems, bypass activation and MPPT correction are often separated both in time and in information content. By contrast, a crossbar-based analog front end can be interpreted as a common computational layer that transforms multiple cell-related observables into several control-relevant outputs simultaneously. This does not guarantee perfect global optimization under every shading profile, but it creates the possibility of responding to local degradation before it has propagated into a larger string-level power loss. In practical terms, this can mean earlier bypass activation, shorter residence time in reverse-bias-prone conditions, reduced

disturbance of the remaining active cells, and faster movement of the converter toward a more favorable operating region. Even when the eventual system still includes slower supervisory logic, the first response to mismatch can be formed much more quickly than in a purely sequential digital loop. For this reason, Figure 6 is intentionally placed in the appendix as a forward-looking application preview. It is meant to suggest why the foundational concepts introduced in this note are not only relevant to in-memory computing and neuromorphic hardware, but may also be important for intelligent power-electronic systems in which energy capture depends on acting rapidly on distributed local information. The possible benefit is not merely lower computational latency in an abstract sense; it is the prospect of converting a greater fraction of time-varying available irradiance into useful electrical output by reducing delay in mismatch handling and by supporting more coordinated control actions. This application perspective is developed more explicitly in the subsequent notes, where the hybrid and fully analog photovoltaic-control architectures are discussed in greater detail.

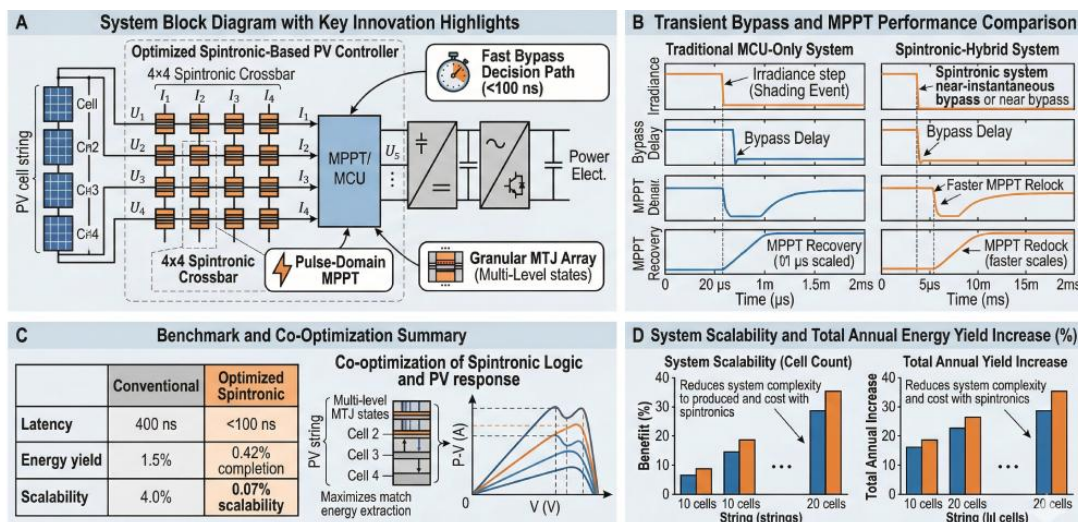


Figure 6: Application-Oriented Overview of a Spintronic-Crossbar-Assisted PV Control Concept. (A) Conceptual System Block Diagram with a 4x4 Spintronic Crossbar and Fast bypass Path. (B) Qualitative Comparison of Transient bypass and MPPT Response Versus a Conventional Digital Approach. (C) Conceptual Benchmark and Co-optimization Summary. (D) Illustrative Scalability and Annual Energy-yield Impact. The Figure is Intended as a System-Level Preview of Later Application Notes and Should not be Interpreted as a Device-Physics Characterization of Multilevel MTJ Switching

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Conflicts of Interest

The author is employed by the company IFEVS and declares that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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 24. See also Ref. 11 for foundational spintronic crossbar-junction patent literature.