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Pulse-Width Modulation Class-D Radio-Frequency Power Amplifier (RF PA)

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Abstract

Power Electronics applications have long employed switching techniques including pulse-width and pulse-density modulation. Because semiconductor technology is growing so quickly, blocks in the radio architecture may benefit from similar strategies. The implementation of a class-D power amplifier for radiofrequency applications in low-GHz frequency bands is described in this paper. We explain why linear amplitude modulation of a nominally nonlinear switching power amplifier is desirable through the use of pulse-density modulation (PDM). With a peak efficiency of 43.5% at 1.95GHz and an output power of up to 20dBm, the amplifier achieves linearity appropriate for wideband wireless standards. The system produces amplitude-modulated waveforms with an envelope bandwidth of up to 20MHz, proving the applicability of this method for contemporary communication standards.

Keywords: Pulse-Density, Semiconductor, Class-D, Amplitude

Introduction

After decades of successful process and technology scaling, active semiconductor devices are now operating with current and power gain-bandwidths (f_t and f_{max}) in excess of 100GHz. This enables efficient operation of deep-submicron CMOS technology at radio frequencies with conventional analog and digital circuitry. In modern digital CMOS technologies, core libraries of standard cells can operate at low-GHz carrier frequencies.

Combined with extraction of layout parasitic, standard-cell design- flow allows direct and rapid synthesis of computational blocks at RF frequencies. This enables complex digital processing and control of RF switching waveforms. Trends in processing speed and circuit design methodology will have a direct impact on many blocks in wireless systems. As this work demonstrates, techniques previously used for audio amplifiers, motor control, and power conversion may now be relevant for RF applications. Here we present an RF power amplifier (RF PA) implemented as a power digital-analog converter (DAC). The class-D PA operates with both NMOS and PMOS complementary devices photo shown in figure 1. We implement digital control of the carrier amplitude using pulse-density modulation (PDM).

Two stages of digital circuitry shape quantization noise away from the signal band. A High-quality factor (Q) passive filter attenuates out-of-band noise, and reduces power loss from harmonics. With appropriate passive components, we achieve unloaded Q in the range of 20-30 in the output network.

Figure 1: Transmitter Modules for pulse-density modulation process driving a class-D PA

Recent generations of polar and envelope tracking (ET) systems as well as traditional linear RF modulators can be replaced by pulse-density amplitude modulation. Polar systems dynamically regulate the RF PA supply voltage, increasing the efficiency of conventional power amplifiers. Wideband spectral richness in the amplitude and phase signals makes polar systems challenging to design and susceptible to AM-AM and AM-PM distortion. Pulse-density modulation increases efficiency at low power levels by scaling switching losses with carrier amplitude. For standards with a high peak-average power ratio (PAPR), this raises average efficiency. Because carrier amplitude is solely a function of pulse density, which the digital system can precisely manage, linearity is also enhanced. The PDM system removes the inherent concerns with AM-AM, AM-PM distortion, and power supply noise by doing away with the necessity for dynamic supply adjustment.

Architecture

Figure 2: depicts the photo RF module, which has a class-D PA, digital upconversion, and two noise shaping stages. A 50% duty cycle pulse waveform is driven by the PA into the corresponding network and bandpass filter. The PDM process functions as an RF-DAC, transforming the baseband signal with a high dynamic range into a 1-bit representation that works at the carrier frequency. The second stage pulse-density modulator is controlled by the noise shaping process of the first-stage /Σ modulator as shown in figure 3. The second stage modulator creates the pulse waveform at the RF carrier frequency using binary codes that have been programmed. The upconversion block mixes the output with the carrier to generate the correct amplitude for the carrier. The PDM process controls the amplitude of the carrier fundamental by changing the density of pulses at the carrier frequency.

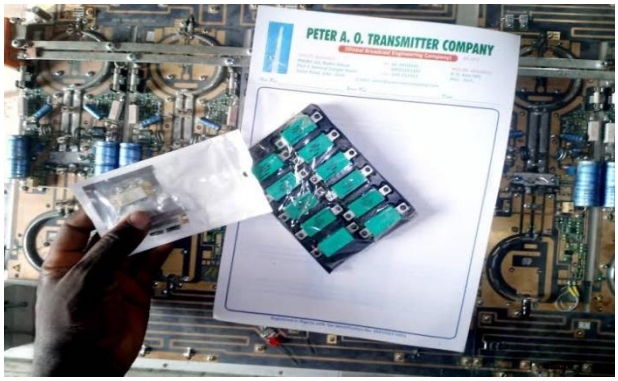

Figure 2: Photo of RF modules for amplitude modulation

The amplitude-modulation-like spectrum is produced by the pulse-density method. Figure 3 illustrates how the output contains symmetrical harmonics around the carrier that may taint the output spectrum. Harmonics may potentially cause the system to lose power. The modulation depth (pulse density) and the output filter's quality factor determine the power distribution in pulse-density modulated waveforms, as was covered in [9]. With a loaded quality factor of Q~12 and a pulse density of 50% (6dB power backoff), the carrier in the case shown in Figure. 2 contains around 95% of the harmonic power. This figure decreases with decreasing pulse density and does not account for loss in active and passive components. To prevent harmonic power from getting to the antenna, the filter is made to be high-impedance out of band. A series resonant L-matching network serves as the first stage filter for the voltage-mode class-D PA. Although parallel resonant filters can also be used, their low impedance at the output harmonics increases power loss.

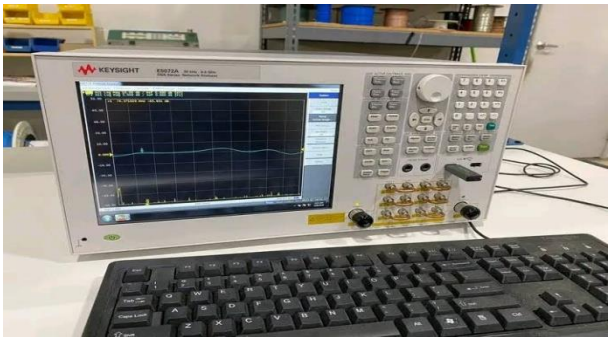

Figure 3: Waveform Error-Feedback Digital ·· Modulator

Numerous procedures that are described in the literature can be digitally applied to create an appropriate noise shaping method. As seen in Figure 4, the RF ouput can be measured.

The 10 quantization levels are converted to a 4-bit representation via a decoder. Out-of-band noise is forced away from the carrier by the programming of the codes. The carrier signal's polarity is indicated by an extra bit. The polarity bit improves linearity as the signal amplitude approaches zero and can be used to reduce the bandwidth of polar amplitude and phase signals.

Figure 4: RF Output wattage measurement

Class-d rf power amplifier

By lowering power loss to reactive parasitic components, class-E and class-F soft-switching approaches increase efficiency under typical circumstances as shown in figure 5. However, they depend on the output network to mould the voltage waveform across the active device, which may result in high voltage stress. The complementary class-D output stage is superior to more conventional topologies in contemporary CMOS processes, which are characterized by quick active devices that are limited by low breakdown voltages. With active PMOS pull-up transistors and a complementary output stage, the drain voltage is a square wave. The topologies of classes E and F are susceptible to changes in the load impedance. Even with an ideal output network, Class-F topologies can only approximate a square wave by blocking various combinations of switching harmonics. These topologies are limited by oxide stress in the active devices because in a real-world scenario, the drain voltage may fluctuate above the supply voltage.

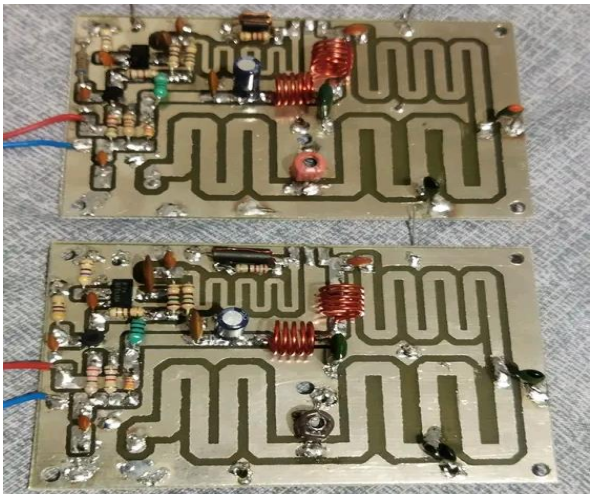

Figure 5: Photo of Class-D Power Amplifier Pallet

In figure 6, two variable resistors are using to control bias of merit are assigned to different switching amplifiers for comparison. Two important figures of merit (FOM) are related to the voltage and current stresses in the device.

Figure 6: Bias Control V_{GS}

Topologies. However, in deep-submicron processes, p- channel devices may have ft in excess of 40GHz [2]. Device scaling further improves operation frequencies and reduces switching losses [1]. In this design the advantage of using a low-impedance complementary.

Amplifier Class	F_V	F_I
E	3.56	1.54
F_{-1}	3.14	1.41
$E/F_{2,3,4,5}$	3.20	1.45
D	2.00	1.57

Table 1: Comparison of FOMs of Various Amplifier Classes (Data for CLASS E, F-1, F2,3,4,5 FROM [12])

Table I compares the class-D topology to other switching-class amplifiers. Oxide stress as a function of supply voltage is lower for class-D, especially compared to class-E. This allows the devices to deliver higher average power to the load for a given peak oxide stress. Since each switch has half-wave sinusoidal drain current, F_I is comparable to the other amplifier topologies. An important advantage of the class-D amplifier is that the output stage is always low impedance. Variation in the impedance of the output network caused by load pull from the antenna does not affect F_I and F_V ratios. This makes the class-D output stage robust against impedance variation compared to other switching amplifier topologies.

The construction of the class-D amplifier module shown in figure 7. This increases capacitance, reducing efficiency compared to NMOS-only output stage outweighs higher losses in the p-channel device.

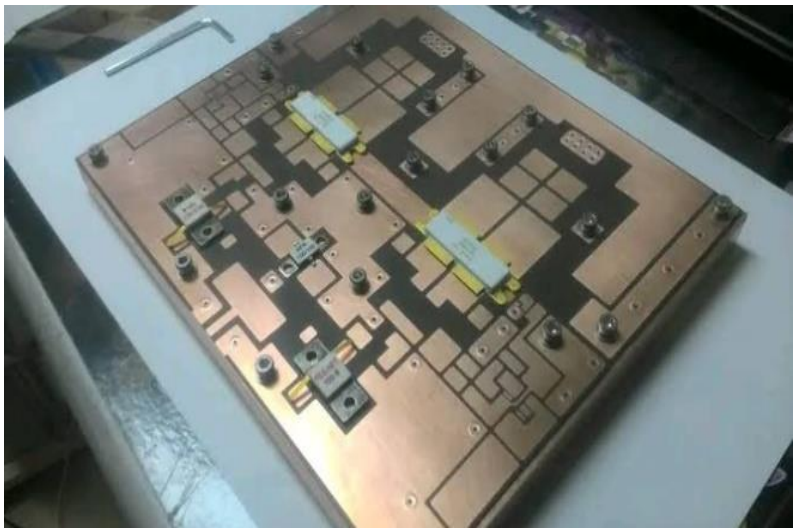

Figure 7: Photo of construction of class-D power amplifier

Affected by pulse-skipping. For class-E or F, the startup time to achieve nominal steady state operation can lead to distortion. This second-order effect is caused by reliance on the output network to shape the drain voltage waveform. Voltage-mode class-D amplifiers force a nearly ideal drain voltage because the switching-node is always low impedance.

Class-D amplifiers are less likely to need pre-distortion to compensate AM-AM and AM-PM distortion than class-E or class-F amplifiers due to inherent open-loop linearity in PDM operation.

Implementation

Figure. 8 shows LPF for the output of the CMOS class-D PA. To achieve higher output power, the output stage uses a cascade device, allowing higher voltage operation. The output devices are thin-oxide transistors with high f_t which can achieve higher efficiency than thick-oxide devices for the same supply voltage. The PA operates with a high voltage rail,

VHV=2.0V, and a center voltage rail, V_{half} =1.0V. The V_{half} node is shared by the high-side and low-side drivers such that current from driving the PMOS output device is reused to drive the NMOS device. Each cascode device was built to share the diffusion region of the switching device in order to reduce parasitic junction capacitance at the cascode node. The finger width for both cascode and switch was 5um to minimize gate resistance.

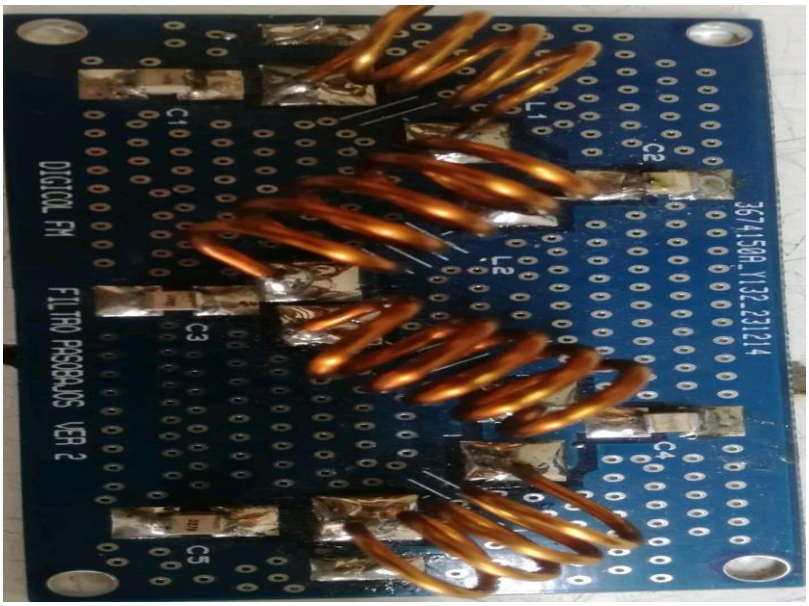

Figure 8: Photo of Low-Pass-Filter (LPF)

The complete unit assembly is shown in figure. 9, is used to interface the nominal 1.0V digital processing block to the PA output devices. Coupling capacitors increase frequency response of the digital signals. Dead time control is implemented with fixed delay of 60ps in the high-side and low-side signal paths. In the dead time circuit, capacitors are placed between the high- side and low-side signals to assure proper time-alignme.

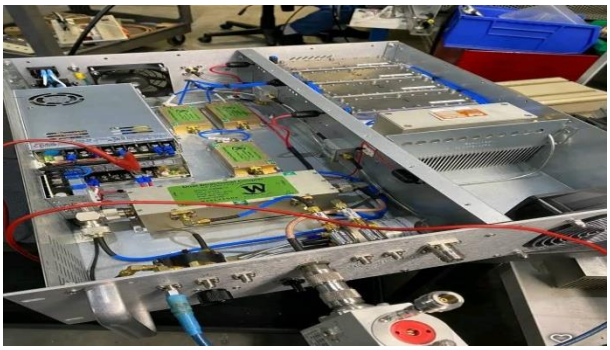

Figure 9. Assembled Amplifier Module

The circuit was implemented in a 90nm digital CMOS test chip. The die photo is shown in figure 11. The class-D PA die is 1.0mmx1.0mm with active area for the PA of 0.15mm^2.

The PDM circuit requires 0.2mm2 active area on a separate test chip that is 1.2mmx1.2mm.

In the future the PA, PDM, and blocks will be integrated. The baseband modulator was implemented on an FPGA clocked at 100MHz. The 1.95GHz RF clock signal is injected directly into the PDM chip with an off-chip RF source. A Lab view PXI system drives the RF clock. The off-chip band pass filter was implemented with a series- resonant L-matching network to transform the 50Ω load impedance to approximately 15Ω. Figure. 10 shows the photo of high-power compound amplification system. Here, the amplitude signal is a full-scale linear ramp. The amplitude is bi-polar as controlled by the polarity bit. The polarity shift is controlled in the amplitude modulator by inverting the phase of the RF clock. The inherent linearity of the system is demonstrated qualitatively by the linearity of the ramp signal. The ramp sweeps between full-scale to zero amplitude in approximately 20us. The efficiency and linearity across the full range of carrier amplitude. The x-axis corresponds to the quantized pulse-density levels in the second stage modulator. The right-hand y-axis shows carrier amplitude as a function of pulse density.

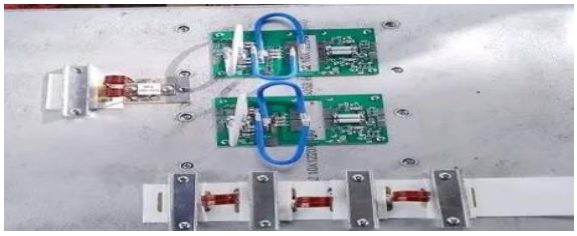

Figure 10: Photo of High-Power Compound Amplification System

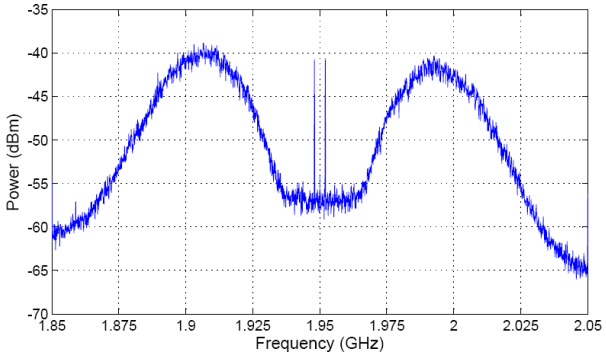

Figure 11: Output spectrum for suppressed-carrier amplitude modulation signal

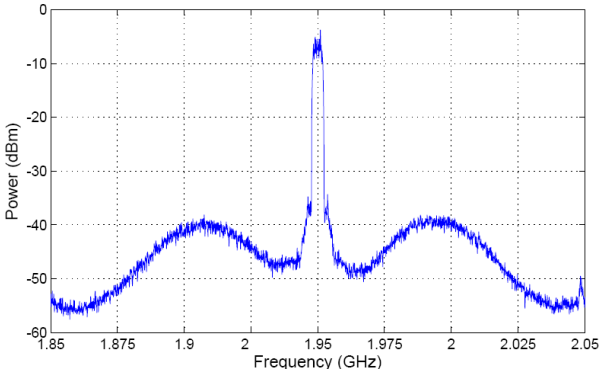

Figure 12: Output Spectrum for WCDMA channel waveform

Carrier amplitude is reduced. The PA achieves 20% efficiency for pulse streams with only 2 out of 9 pulses delivered (13dB power backoff). High efficiency in power back off improves the average efficiency of the system for wireless standards with high peak-average power ratios (PAPR). High linearity is achieved with the PDM scheme as measured in terms of carrier amplitude versus pulse density. Figure 11 shows the output spectrum of the PA driving a suppressed-carrier amplitude modulation signal. The AM signal has 20mV amplitude with zero DC component to suppress the carrier tone. This plot highlights the low- amplitude noise-shaping performance of the modulator. Near-band noise is suppressed substantially by the modulator. Peak noise occurs 50MHz on either side of the carrier frequency. Figure 12 shows the spectrum at the PA output for a WCDMA channel waveform. The signal is analogous to a single I or Q signal from the Cartesian representation. It is band limited to 3.84MHz with a PAPR of approximately 3.0dB. Peak noise occurs approximately 50MHz from the carrier. The bandwidth of the system is limited by the baseband sampling rate of 100MHz. With this sample rate the system can accurately generate waveforms with over 20MHz channel bandwidth. The out-of-band quantization noise is the limiting factor for the pulse-density modulation system.

Although this system successfully reconstructs the RF channel waveforms, the WCDMA waveform's noise level is insufficient to satisfy the standard's spectral-mask requirements.

To further decrease out-of-band noise, more investigation is required. By running the baseband noise-shaping at higher frequencies, noise can be minimized. In a fully integrated solution, it would be practical to operate the process at 250MHz or more, which would reduce the peak noise level by up to 10dB, depending on the attenuation of the bandpass filter. Another approach is to power combine multiple PA outputs to add additional quantization levels for the digital modulator. Peak out-of-band noise is decreased and the signal-noise ratio is directly improved with more bits. Another possibility is higher-order filters. MEMS and acoustic devices are examples of discrete band pass filter components that may offer significant attenuation for out-of-band noise, making the PDM system suitable for a variety of wireless standards. Other wireless technologies, like Bluetooth, might present a chance because low-power systems' spectrum requirements are more adaptable.

Conclusion

All things considered, this work presents a novel approach to the transmitter architecture that blends methods from RF circuit design, data conversion, and power management. The 90nm CMOS test chip uses pulse-density modulation to linearly modulate a nonlinear amplifier. Wideband RF amplitude waveforms can be produced using the digital design, which also achieves excellent linearity and high efficiency over a broad range of output power. Even with losses in the off-chip matching network and PA driver power, the class-D PA has an efficiency of 43.5% at 1.95GHz. By using a deterministic pulse-density modulation technique at the RF carrier frequency, the architecture takes advantage of technology scaling. This study demonstrates that methods effectively created for power electronics applications apply to radio architectural blocks.

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